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EXAMINER	
JOHNSON, BRIAN P	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,803	BARRY ET AL.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-19,22 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-19, 22, and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 9-19, 22, and 28-30 are pending.

Papers Filed

2. Examiner acknowledges receipt of amendments and remarks filed 04 August 2008.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first and paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
>
> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 29 and 30 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In particular, there is no stage that can be described as single-cycle. See fig. 9B.

6. Claims 5, 9, and 28-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 29 and 30, since Applicant has attempted to redefine the word “cycle” in such a way that PCLK cycles can contain multiple MCLK cycles, then this must be made clear in the claims. To say a stage is single cycle when it contains multiple MCLK cycles is misleading.

Regarding claims 5, 9, and 28, latency, according to Applicant, is a term associated with an instruction. To refer to the "latency of an adaptable decode stage" doesn't really make sense. Applicant is referring to the duration of a decode stage. Language, for example, like that of claim 19 is more appropriate: "wherein each stage of the normal pipeline has a duration equal to the first execution latency.”

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 9-12 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowell (U.S. Patent No. 3,623,017) in view of Kurshid (U.S. Publication No. 2002/0104032)

7. As per claim 1, Lowell teaches a processor with an instruction class controllable pipeline comprising:

a program storage unit (Fig. 1 memory unit 18) holding a diverse plurality of class one and class two executable function instructions, the class one instructions having a first execution latency and the class two instructions having a second execution latency, wherein the first execution latency is shorter than the second execution latency; (Col. 1 lines 5-25)

a fetch stage for fetching an instruction from the program storage unit to be stored in an instruction register; (Fig. 1 instruction register 28)

a decode stage for classifying and decoding the instruction stored in the instruction register, and generating an instruction class indication and storing the decoded instruction in a decode register; (Fig. 1 decoder 30)

an adaptable pipeline control unit responsive to the instruction class indication for adapting the latency of a pipeline stage dependent to the instruction class; (Col. 1 lines 5-25)

and an adaptable execution stage operable for execution of a decoded instruction stored in the decode register, the decoded instruction being a class one instruction or a class two instruction. (Fig. 1 arithmetic section 14)

Lowell fails to disclose that the decode and fetch unit are adaptable based on latency.

Kurshid shows a different technique of adapting the functional units clock (paragraph 21) based on instruction latency (paragraph 22), which affects the CPU clock causing the fetch and decode stage to be adaptable (paragraphs 27-30; fig. 2).

Lowell would have been motivated to utilize the technique of Khurshid to prevent stalls and save power based (Kurshid paragraph 7).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Lowell and incorporate the teachings of Kurshid in such a way that the extended clock affects the CPU clock making the fetch and decode stages adaptable based on instruction latency.

8. As per claim 2, Lowell/Kurshid teaches the processor of claim 1, wherein the fetch stage further comprises: a program counter and an instruction memory fetch mechanism which are operable to begin instruction processing by fetching one or more instructions from the program storage unit. *Fig. 1 discloses using program counter 26 to index into memory 18 to obtain the instruction held in instruction register 28.*

9. As per claim 3, Lowell/Kurshid teaches the processor of claim 1, wherein the executable function instructions comprise: additions, subtractions, multiplications, divisions, compares, ANDS, ORs, ExclusiveORs, NOTs, shifts, rotates, permutes, bit

operations, moves, loads, stores, communications or combinations thereof. *Lowell discloses multiply, and divide (col. 1 line 9).*

10. As per claim 4, Lowell/Kurshid teaches the processor of claim 1, wherein the adaptable pipeline control unit further comprises: a pipeline control mechanism for class one instructions to execute in a instructions having a first execution latency; and a pipeline control mechanism for class two instructions to execute in instructions having the first execution latency. *Lowell col. 1 lines 5-20 teaches passing non-extended sequence instructions through the pipeline in a typical fashion and pausing the front end of the pipeline for the arithmetic hold condition (class two instruction).*

11. As per claim 5, Lowell/Kurshid teaches the processor of claim 4 wherein the pipeline control mechanism for class one instructions further comprises: control for normal pipeline timing for class one instructions wherein each stage of the normal pipeline has a duration equal to the first execution latency. *Lowell col. 1 lines 5-20 teaches passing non-extended sequence instructions through the pipeline in a typical fashion.*

12. As per claim 9, Lowell/Kurshid teaches the processor of claim 1 wherein the adaptable execution stage further comprises: a class one execution unit operable to execute a class one instruction stored in the decode register, wherein the class one execution unit has the first execution latency; and a class two execution unit operable to

execute a class two instruction stored in the decode register, wherein the class two execution unit has the second execution latency. (Fig. 14 arithmetic unit 14)

13. As per claim 10, Lowell/Kurshid teaches the processor of claim 1 wherein the decode stage further operates to decode an opcode field to classify an instruction. *Since certain instructions are deemed to be "extended sequence instructions", and the processor goes into an arithmetic hold for these instructions (col. 1 lines 5-25) there must exist decode circuitry to classify these instructions as class two instructions based on instruction type. An opcode inherently defines the function an instruction is perform.*

14. As per claim 11, Lowell/Kurshid teaches the processor of claim 1 wherein the decode stage further operates to decode an opcode field and decode of a data type field to classify an instruction. *The examiner asserts that the opcode field is a data field and indicates what type of instruction to perform.*

15. As per claim 12, Lowell/Kurshid teaches the processor of claim 4 wherein the adaptable pipeline control unit further comprises:

a programmable clock gating mode indicator that specifies a normal clock gating mode and a slow down clock gating mode;

and control for extending pipeline sequencing both class 1 instructions and class 2 instructions to execute in a third longer time period when the programmable clock gating mode indicator specifies a slow down clock gating mode. *Lowell teaches that a*

slower clock will execute both extended and non-extended instructions. Inherently, executing both a class 1 and a class 2 instruction in the slower clock would take a longer time than executing either alone in either the same or the faster clock.

16. Regarding claim 28, Lowell/Kurshid discloses the processor of claim 1 wherein the latency of the adaptable fetch stage and the latency of the adaptable decode stage are both set equal to the latency of the instruction that is executing the adaptable execution stage (Kurshid paragraphs 27-30; fig. 2).

17. Regarding claim 29, Lowell/Kurshid discloses the processor of claim 1 wherein the adaptable execution stage is a variable duration single-cycle execution nstage having a first duration of execution equal to the first execution latency for executing class one instructions and having a second duration of execution equal to the second execution latency for executing class two instructions (Kurshid paragraphs 27-30; fig.2)

18. Regarding claim 30, Lowell/Kurshid discloses a processor with an instruction class controllable execution pipeline comprising:

an instruction register for holding a class one instruction or a class two instruction, the class one instruction belongs to a first group of diverse class one instructions that execute in a time that is less than or equal to a first time period, the class two instruction belongs to a second group of diverse class two instructions that execute in a time that is less than or equal to a second time period (col 1 lines 5-25), the

first single-cycle time period is shorter than the second single-cycle time period (col 1 lines 5-25); an adaptable (Kurshid paragraphs 27-30; fig. 2) decode stage for classifying and decoding the instruction stored in the instruction register, generating an instruction class indication representing the instruction class of the instruction receive in the instruction register, and storing a decoded instruction in a decode register (col 1 lines 5-25); an adaptable (Kurshid paragraphs 27-30; fig. 2) execution stage responsive to execute a decoded instruction stored in the decode register, the adaptable execution stage having a first execution logic unit for executing instructions of the first group, a second execution logic unit for executing instructions of the second group (col 1 lines 50-55); and an adaptable pipeline control unit responsive to the instruction class indication for adapting the time period of the adaptable decode stage and the adaptable execution stage for decoding and executing an instruction in the first time period for class one instructions and in the second time period for class two instructions dependant on the instruction class indication (col 1 lines 5-25).

19. Claims 6, 7, and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowell/Kurshid in view of Official Notice.

20. As per claim 6, Lowell/Kurshid teaches the processor of claim 4 wherein the pipeline control mechanism for class two instructions further comprises a method for holding values of the instruction register, decode register and program counter upon detection of a class two instruction. *Inherently, there must exist signals to each of these*

registers to signify the "arithmetic hold" condition (Lowell Col. 1 lines 5-25) and a control for extending pipeline sequencing for class two instruction to execute in a second longer time period. *(Lowell Col. 1 lines 5-25)*

21. Lowell/Kurshid fails to disclose an instruction register feedback multiplexer; a decode register feedback multiplexer; a program counter and program counter update function;

22. Official Notice is taken that feeding back a register to itself by means of a multiplexer is well known in the art. It provides a low-cost, simple implementation of retaining a register's contents by means of a control line selecting either the current value or a new value to be latched into the register.

23. It would have been obvious to one of ordinary skill in the art at the time of invention to have implemented feedback multiplexers to retain the values of the instruction register, decode register and program counter upon detection of an arithmetic hold for the benefit of a low-cost, simple implementation.

24. As per claim 7, Lowell/Kurshid teaches the processor of claim 4 wherein the pipeline control mechanism for class two instructions further comprises a method for holding values of the instruction register, decode register and program counter upon detection of a class two instruction. *Inherently, there must exist signals to each of these registers to signify the "arithmetic hold" condition (Lowell Col. 1 lines 5-25)* and control for extending pipeline sequencing for class two instructions to execute in a second longer time period. (Col. 1 lines 5-25)

25. Lowell/Kurshid fails to disclose an instruction register gated clock; a decode register gated clock; a program counter gated clock;

26. Official Notice is taken that shutting off the clock to a register by means of a simple AND gate is well known in the art. "Clock Gating" provides the benefit of a very simple, low-cost method of forcing a register to retain its current value.

27. It would have been obvious to one of ordinary skill in the art at the time of invention to have implemented a gated clock to the instruction register, decode register and program counter register as the means of retaining their values during an arithmetic hold for the benefit of low-cost, simple implementation.

28. As per claim 13, Lowell/Kurshid teaches a method for processor performance and power optimization of an instruction class adaptable pipeline processor supporting at least two classes of instructions with a first class operable at a with a first latency for each pipeline stage of the adaptable pipeline and a second class operable with a second latency for each pipeline stage and where, the first latency is shorter than the

second latency and where the instructions operable with the first latency can be specified to operate with the first latency or with the second latency and where the instructions operable with the second latency can be specified to only operate with the second latency, the method comprising:

programming the instruction class adaptable pipeline processor creating an application program containing a mix of two classes of instructions to meet functional requirements with a first plurality of instructions used in the program operable with the first latency specified in a formation of each of the first plurality of instructions as class 1 instructions; *The examiner asserts that the "extended sequence instructions" (class 1 instructions) are specified to operate at a faster frequency (col. 1 lines 5-25).*

29. Lowell/Kurshid fails to disclose modifying the application program to meet performance and power requirements of an application by changing, where appropriate, class 1 instructions to class 2 instructions.

30. Official Notice is taken that complex instructions can be changed to simpler microinstructions for the purpose of quicker execution.

31. It would have been obvious to one of ordinary skill in the art at the time of invention to allow Lowell/Kurshid's invention to be simplified by using microinstructions that are more easily executed by the processor.

32. As per claim 14, Lowell/Kurshid discloses a method for processor performance and power optimization of claim 13 wherein modifying the application program to meet

performance and power requirements of an application, Lowell/Kurshid fails to disclose the method further comprising:

appropriately programming a programmable clock gating mode to cause a specifiable majority of the instructions of the class adaptable pipeline processor to execute at a longer latency than the second latency associated with the class 2 instructions.

Official Notice is taken that slowing down a clock for purposes of reducing power consumption is well known in the art.

33. It would have been obvious to one of ordinary skill in the art at the time of invention to have specified, for all instructions, to slow the processor's clock to a slower speed for the benefit of conserving power.

34. Claims 15-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowell/Kurshid (U.S. Patent No. 3,623,017) in view of Ishikawa (U.S. Patent No. 5,787,303).

35. As per claim 15, Lowell/Kurshid teaches a processor with an instruction class controllable pipeline comprising:

a program storage unit (Fig. 1 memory unit 18) holding a diverse plurality of class one and class two executable function instructions, the class one instructions having a shorter execution latency and the class two instructions having a longer execution latency; (Col. 1 lines 5-25)

a fetch stage for fetching an instruction from the program storage unit to be stored in an instruction register; (Fig. 1 instruction register 28)

a decode stage for classifying and decoding the instruction stored in the instruction register, and generating an instruction class indication and storing the decoded instruction in a decode register; (Fig. 1 decoder 30)

an adaptable pipeline control unit responsive to the instruction class indication for adapting the pipeline latency of each stage of the plurality of instruction class controllable pipelines dependent on the instruction class instructions; (Col. 1 lines 5-25)

and an adaptable execution stage operable for execution of a decoded instruction stored in the decode register, the decoded instruction being a class one instruction or a class two instruction. (Fig. 1 arithmetic section 14)

36. Lowell/Kurshid fails to teach whereby the system is configured for VLIW processing.

37. Ishikawa teaches a processor for executing VLIW instructions.

38. Ishikawa teaches that VLIW processing decreases a processor's CPI, increasing the throughput. (Col. 1 lines 10-52)

39. It would have been obvious to one of ordinary skill in the art at the time of invention to have modified Lowell/Kurshid's processor to handle VLIW instructions by

reproducing the instruction pipeline in parallel for the benefit of increased instruction throughput.

40. As per claim 16, Lowell/Kurshid and Ishikawa teach the VLIW processor of claim 15, wherein the VLIW fetch stage further comprises: a VLIW memory control unit which is operable to begin VLIW processing by fetching a VLIW from the VLIW storage unit. *The examiner asserts that Lowell and Ishikawa's processor must inherently fetch an instruction word from memory before being able to operate on it. Inherently, there must exist circuitry to control this memory access.*

41. As per claim 17, Lowell/Kurshid and Ishikawa teach the processor of claim 15, wherein the executable function instructions comprise: additions, subtractions, multiplications, divisions, compares, ANDS, ORs, ExclusiveORs, NOTs, shifts, rotates, permutes, bit operations, moves, loads, stores, communications and variations or combinations thereof; *Lowell discloses multiply, and divide (col. 1 line 9).*

42. As per claim 18, Lowell/Kurshid and Ishikawa teach the processor of claim 15, wherein the adaptable pipeline control unit further comprises:

a pipeline control mechanism for a VLIW, consisting of all class one instructions, to control the execution of the VLIW with the first execution latency; *Lowell col. 1 lines 5-20 teaches passing non-extended sequence instructions through the pipeline in a typical fashion.*

and a pipeline control mechanism for a VLIW, consisting of at least one class two instruction, to control the execution of the VLIW with the second execution latency. (*Lowell col. 1 lines 5-20)*

43. As per claim 19, Lowell/Kurshid and Ishikawa teach the processor of claim l 8 wherein the pipeline control mechanism for a VLIW consisting of all class one instructions further comprises: control for normal pipeline timing for the class one instructions wherein each stage of the normal pipeline has a duration equal to the first execution latency. *Lowell col. 1 lines 5-20 teaches passing non-extended sequence instructions through the pipeline in a typical fashion.*

44. As per claim 22, Lowell/Kurshid and Ishikawa teach the processor of claim 15 wherein each adaptable execution stage of the plurality of adaptable execution stages further comprises: a class one execution unit operable to execute a class one instruction stored in the decode register, wherein the class one execution unit has the first execution latency; and a class two execution unit operable to execute a class two instruction stored in the decode register, wherein the class two execution unit has the second execution latency. (*Ishikawa Fig. 9)*

Response to Arguments

45. Applicant's arguments with respect to claims 28-30 are persuasive. These claims were not appropriately addressed in the previous action. Consequently, this

action is made Non-Final to allow Applicant an opportunity to respond to these claim rejections. Further changes have also been made to the rejection of claim 13 in light of Applicant's arguments.

Applicant's other arguments, however, are not persuasive.

46. Applicant argues that "Lowell does not teach and does not make obvious classifying an instruction based on an instruction's execution latency to generate an instruction class indication." This argument is without merit. Lowell discusses normal and extended sequence instructions. So, separate classes of instructions are distinguished. The only question left to determine is whether this classification is based on latency.

Applicant states that "The execution latency of an instruction 'is measured by each instruction's critical path, a measure of the worst-case signal propagation time for the instruction in each pipeline stage.'" See Page 6 of the Remarks. This "definition," as Applicant appears to argue, provides the appropriate amount of weight to be given to the word "latency" when it is read in light of the specification. Applicant's statement, however, is a blatant mischaracterization of the specification. Applicant cites page 6 lines 18-23 of the Specification for this definition. The citation states, "<u>[i]nstruction timing performance</u> is measured by each instruction's critical path, a measure of the worst-case signal propagation time for the instruction in each pipeline stage." (emphasis added) There is <u>nothing</u> in the page that even mentions the word latency. Applicant's apparent suggestion that the word latency should properly be given this definition when read in light of the specification is entirely misleading.

In fact, it is entirely reasonable for Lowell's "extended sequence instructions" which are distinguished based on "a relatively long execution time" to be interpreted as "based on an instruction's execution latency."

Conclusion

47. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Perry et al. (U.S. Patent No. 5,142,684) disclose a system of slowing a processor clock when power consumption requirements dictate to do so.

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183